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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,522	07/08/2003	Jeremy A. Theil	10021136-1	9342

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EXAMINER	
SELBY, GEVELL V	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,522	THEIL ET AL.	
	Examiner	Art Unit	
	Gevell Selby	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claim 10 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 10 depends on itself. For examination purposes, claim 10 will changed to amend from claim 1.

3. Claims 11-17 are objected to for depending from claim 10 that was objected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3 and 9-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhao et al., US 6,727,946.

In regard to claim 1, Zhao et al., US 6,727,946, discloses an image sensor, comprising:

multiple pixels (CMOS array) each include a respective photodiode region (see figure column 1, lines 7-9);

pixel circuits (see figure 4) each operable to control integration and readout steps for a respective pixel (see column 4, lines 34-64 and column 5, line 65 to column 6, line 3); and

a bias circuit (see figure 4, element 320) operable to apply voltages across the pixels to induce carrier injection into the photodiode regions to reduce image lag (see column 5, line 65 to column 6, line 14).

In regard to claim 2, Zhao et al., US 6,727,946, discloses the image sensor of claim 1, wherein it is inherent the Zhao reference discloses the bias circuit (see figure 4, element 320) is operable to induce forward bias flow of injected carriers through the pixel photodiode regions, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 3, Zhao et al., US 6,727,946, discloses the image sensor of claim 2, wherein it is inherent the Zhao reference discloses the bias circuit is operable to periodically induce forward bias flow of injected carriers through photodiode regions, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 9, Zhao et al., US 6,727,946, discloses the image sensor of claim 1, wherein it is inherent the Zhao reference discloses that the bias circuit is operable to induce carrier injection between photodiode regions of pixels, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 10, Zhao et al., US 6,727,946, discloses the image sensor of claim 1, wherein it is inherent the Zhao reference discloses that the bias circuit is operable to induce carrier injection between photodiode regions of adjacent pixels, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 11, Zhao et al., US 6,727,946, discloses the image sensor of claim 10, wherein it is inherent the Zhao reference discloses that the bias circuit is operable to apply different voltages levels to nodes of adjacent pixels, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 12, Zhao et al., US 6,727,946, discloses the image sensor of claim 11, wherein it is inherent the Zhao reference discloses that the bias circuit is operable to apply different high-to-low voltage ranges across adjacent pixels, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 13, Zhao et al., US 6,727,946, discloses the image of sensor of claim 11, wherein pixels are arranged in an array of multiple rows (ROW: row selection switch to switch between multiple rows) and it is inherent

the Zhao reference discloses that the bias circuit is operable to apply different voltage levels to nodes of adjacent pixels in adjacent rows, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 14, Zhao et al., US 6,727,946, discloses the image sensor of claim 11, wherein pixels are arranged in an array of rows (ROW: row selection switch to switch between multiple rows) and columns (COL: column selection switch to switch between multiple columns) and it is inherent the Zhao reference discloses that the bias circuit is operable to apply different voltage levels to nodes adjacent pixels in adjacent rows and to apply different voltage levels to nodes of adjacent pixels in adjacent columns, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 15, Zhao et al., US 6,727,946, discloses the image sensor of claim 10, wherein the different voltage levels applied to nodes of adjacent pixels are switched periodically (see figure 6F: the V_{RST} is switch on and off periodically).

In regard to claim 16, Zhao et al., US 6,727,946, discloses the image sensor of claim 10, wherein the bias circuit includes two bias lines for applying different respective voltage levels to the pixels (see figure 4, elements BIAS and BCTL).

6. Claims 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Chi, US 5,854,100.

In regard to claim 18, Chi, US 5,854,100, discloses a method of operating an image sensor comprising multiple pixels each including a respective photodiode region (see figure 6a, b, and c), the method comprising:

resetting photodiode regions (see column 7, lines 55-59);

integrating charge in photodiode regions (see column 7, line 60 to column 8, line 2);

sampling pixel nodes (see column 7, line 60 to column 8, line 2); and

inducing carrier injection into photodiode regions to reduce image lag (see column 8, lines 3-15).

In regard to claim 19, Chi, US 5,854,100, discloses the method of claim 18, wherein inducing carrier injection comprises inducing forward bias flow of carriers through the pixel photodiode regions (see column 6, line 64 to column 7, line 10).

In regard to claim 20, Chi, US 5,854,100, discloses the method of claim 18, wherein inducing carrier injection comprises inducing carrier injection between photodiode regions of adjacent pixels (see column 8, lines 3-15).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being obvious over Zhao et al., US 6,727,946, in view of Chi, US 5,854,100.

In regard to claim 4, Zhao et al., US 6,727,946, discloses the image sensor of claim 3. The Zhao reference does not disclose wherein the pixel circuits and the bias circuit are cooperatively configured so that forward bias flow of injected carriers occurs during a reset step for each pixel.

Chi US 5,854,100, discloses a system and method for reducing image lag wherein the pixel circuits and the bias circuit are cooperatively configured so that forward bias flow of injected carriers occurs during a reset step for each pixel (see column 6, line 65 to column 7, line 21 and line 55 to column 8, line 15).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Zhao et al., US 6,727,946, in view of Chi US 5,854,100, wherein the pixel circuits and the bias circuit are cooperatively configured so that forward bias flow of injected carriers occurs during a reset step for each pixel, in order to reduce the effects of electric charge charged in the photo-detector, thus reducing the image lag.

In regard to claim 5, Zhao et al., US 6,727,946, in view of Chi US 5,854,100, discloses the image sensor of claim 2. The Chi reference discloses wherein pixels are arranged in an array of multiple rows and the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through

the photodiode regions of all pixels in a given row of the array (see column 6, line 65 to column 7, line 21).

In regard to claim 6, Zhao et al., US 6,727,946, in view of Chi US 5,854,100, discloses the image sensor of claim 5. It is implied the bias circuit of the Zhao reference is operable to simultaneously induce forward bias flow of injected carriers through the photodiode regions one row at a time, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 7, Zhao et al., US 6,727,946, in view of Chi US 5,854,100, discloses the image sensor of claim 6. It is implied the bias circuit of the Zhao reference is operable to simultaneously induce forward bias flow of injected carriers through photodiode regions of a given row before the pixel circuits in the given row initiate an integration step for the given row, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 8, Zhao et al., US 6,727,946, in view of Chi US 5,854,100, discloses the image sensor of claim 5. It is implied the bias circuit of the Zhao reference is operable to simultaneously induce forward bias flow of injected carriers through photodiode regions of all rows in the array, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being obvious over Zhao et al., US 6,727,946, in view of Baer, US 6,914,230,

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

In regard to claim 17, Zhao et al., US 6,727,946, discloses the image sensor of claim 10, wherein the bias circuit includes a bias line (see figure 4, element BIAS). The Zhao reference does not discloses the component of the bias circuit.

Baer, US 6,914,230, discloses a system and method for reducing image lag wherein the bias circuit comprises a set of resistive elements respectively coupled in parallel between the bias line and alternate pixels (see figure 5, element 108 and 112).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Zhao et al., US 6,727,946, in view of Baer, US 6,914,230, wherein the bias circuit comprises a set of resistive elements respectively coupled in parallel between the bias line and alternate pixels, in order to reduce the effects of electric charge charged in the photo-detector, thus reducing the image lag.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,229,191, discloses an image sensor with guard rings that prevent image lag.

US 5,614,740, discloses an image sensor with a bias circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gevell Selby whose telephone number is 571-272-7369. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on 571-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

gvs

TUAN HO
PRIMARY EXAMINER